NXP Semiconductors
User Guide

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Smart Access Solution Hardware Developer Guide

Contents

Chapter 1
Introduction

This document is a Hardware Developer's Guide for the Smart Access Platform. NXP Semiconductors fully supports this platform. The Hardware Developer Guide describes advanced system setup and debugging. It provides detailed information on the overall design and usage of the Smart Access Platform from a hardware systems perspective as well as recommended optimization for specific customer products.

1.1 Platform overview

The Smart Access platform is designed to provide a complete hardware and software reference for Smart Access/Lock applications. The Smart Access platform integrates not only basic but also advanced smart lock control methods, such as fingerprint, password, Matter, UWB, Face Recognition. It also provides an HMI interface and voice prompt function. The dedicated NXP element provides security for the system.

The Smart Access platform features and functions lists the features and functions of the Smart Access platform.

The main functions and modules of the Smart Access platform shows the main functions and modules of the Smart Access platform.

Table 1. The Smart Access platform features and functions

Feature	Functions
Smart Access Main System Control	• Main access control, sensor aggregation • HMI interface, voice prompt • Fingerprint matching algorithm • Low-power management
Matter Access Control	• Matter over Thread • Access control through App / Matter gateway
UWB Access Control	• Access control through UWB phone • Optional BLE wake-up
Face Recognition Access Control	• Based on the NXP SLN-VIZN3D-IOTturnkey solution • 3D secure face recognition • Optional 2D secure and low-cost face recognition • Optional video intercom through cloud
Others	• NFC, BLE, pin pad access control • Secure data management

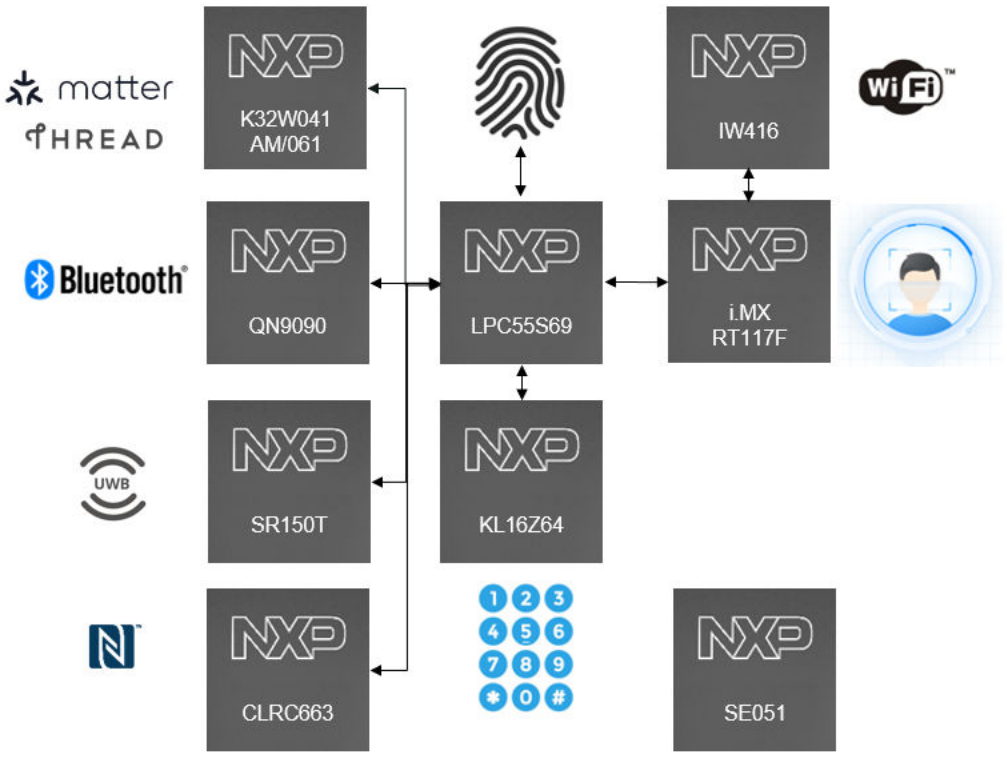


Figure 1. The main functions and modules of the Smart Access platform

The Smart Access platform consists of several boards, each of which communicates with the main board and receives commands to perform its own independent function. These boards and the external modules were carefully selected to achieve optimum performances, low-power capabilities, and competitive cost in production. The scalable platform showcases all NXP smart access technologies and enables faster productization.

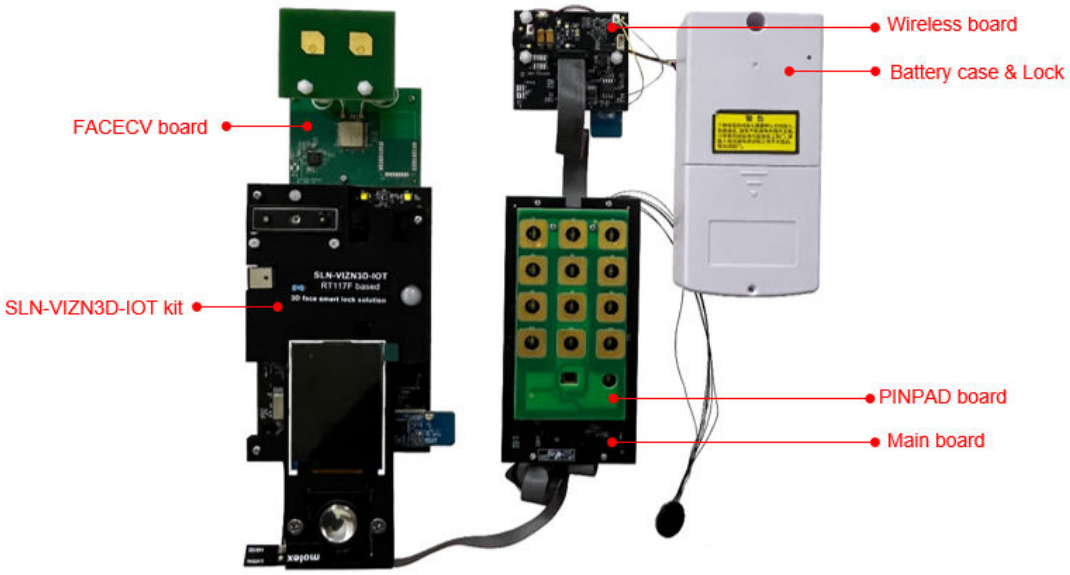


Figure 2. The Smart Access platform

1.2 Smart Access platform revision history

Revision A: Product launch

1.3 Smart Access platform contents

The Smart Access Platform is composed of the following items:

- The Wireless board
- The Main board
- The PINPAD board
- The SLN-VIZN3D-IOT kit
- The FACECV board
- The fingerprint module
- Battery case and Lock

1.4 Smart Access platform design files

The schematics, layout files, and gerber files (including silkscreen) can be downloaded from the NXP Smart Access website. The documentation and design files of the SLN-VIZN3D-IOT kit can be downloaded from the SLN-VIZN3D-IOT Product Support Page on www.nxp.com/mcu_vision3d.

Chapter 2
Main board

The main board based on LPC55S69 acts as a host MCU in the Smart Access Platform, it communicates with other boards to control the door lock in various ways. The pictures of the main board are shown below.

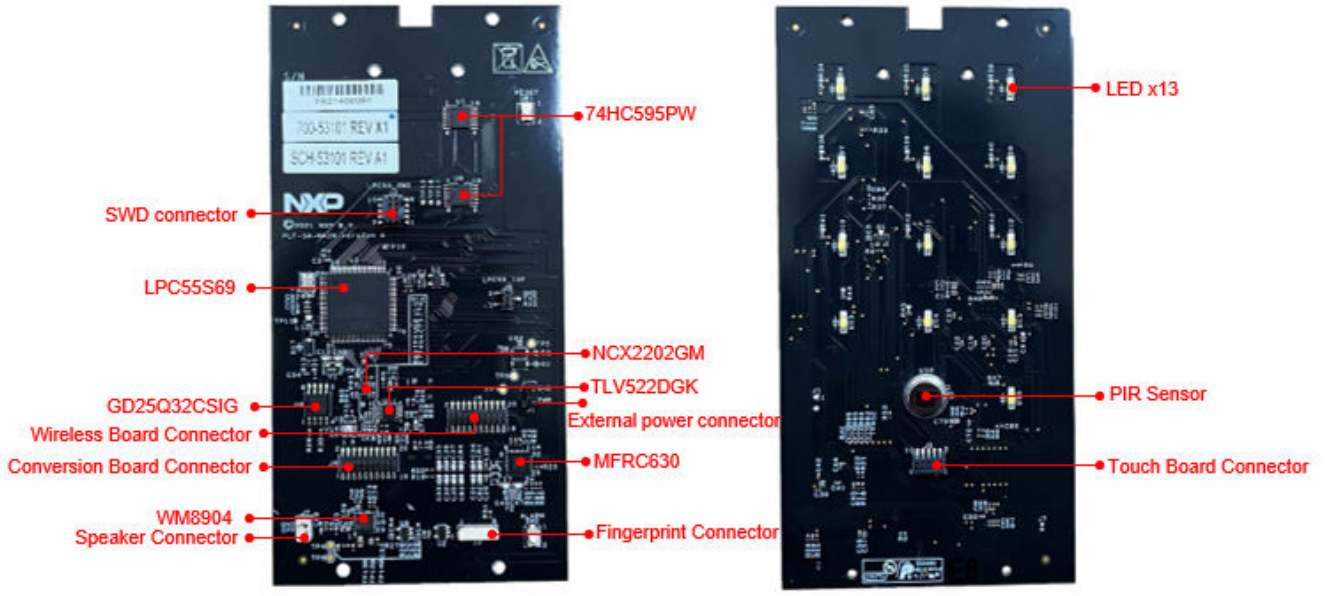


Figure 3. The main board callout

2.1 LPC55S69 microcontroller

The LPC55S6x MCU family is part of the EdgeVerse™ edge computing platform and builds on the world's first general-purpose Cortex-M33-based microcontroller introduced with the LPC5500 series. This high-efficiency family leverages the new Armv8-M architecture to introduce new levels of performance and advanced security capabilities including TrustZone-M and coprocessor extensions.

The LPC55S69 includes an ARM Cortex-M33 coprocessor, CASPER Crypto/FFT engine, PowerQuad hardware accelerator for DSP functions, up to 320 KB of on-chip SRAM, up to 640 KB on-chip flash, PRINCE module for on-the-fly flash encryption/decryption, high-speed and full-speed USB host and device interface with the crystal-less operation for full-speed, SD/MMC/SDIO interface, five general-purpose timers, one SCTimer/PWM, one RTC/alarm timer, one 24-bit Multi-Rate Timer (MRT), a Windowed Watchdog Timer (WWDT), nine flexible serial communication peripherals (which can be configured as a USART, SPI, high-speed SPI, I2C, or I2S interface), Programmable Logic Unit (PLU), one 16-bit 1.0 Msamples/sec ADC capable of simultaneous conversions.

2.2 Memories

One 32 Mbit/4 MB serial SPI NOR flash memory GigaDevice GD25Q32C is connected to the LPC55S69 MCU through its High-Speed SPI interface in standard SPI mode. This external memory stores audio files as well as other files.

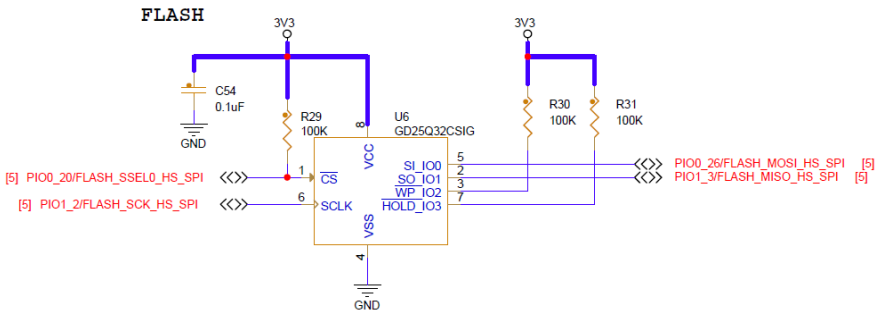


Figure 4. GD25Q32C SPI NOR flash

Table 2. GD25Q32C pin allocation in Smart Access platform

GD25Q32C pin	LPC55S69 peripheral (pin)	Schematic net name
SCLK	PIO1_2	PIO1_2/FLASH_SCK_HS_SPI
CS	PIO0_20	PIO0_20/FLASH_SSEL0_HS_SPI
SI_IO0	PIO0_26	PIO0_26/FLASH_MOSI_HS_SPI
SO_IO1	PIO1_3	PIO1_3/FLASH_MISO_HS_SPI

2.3 Security

The main board embeds an NXP SE051H security element, which supports applet updates in the field and delivers proven security certified to CC EAL 6+, with AVA_VAN.5 up to the OS level. It is connected to the LPC55S69 MCU through the I2C1 interface, as well as a GPIO for Enable/Disable. It can be connected to the other two I2C1 pins of the LPC55S69 by modifying the circuit.

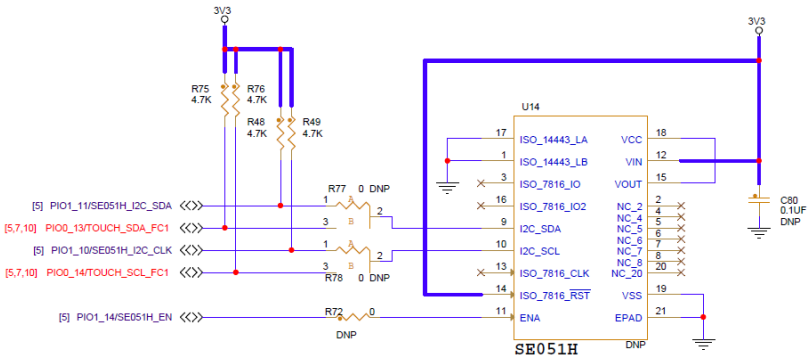


Figure 5. SE051H security element on the main board

Table 3. SE051H pin allocation in Smart Access platform

SE051H pin	LPC55S69 peripheral (pin)	Schematic net name
ENA	PIO1_14/ACMP0_D	PIO1_14/SE051H_EN
I2C_SDA	PIO1_11, PIO0_13	PIO1_11/SE051H_I2C_SDA,

Table continues on the next page...

Table 3. SE051H pin allocation in Smart Access platform (continued)

SE051H pin	LPC55S69 peripheral (pin)	Schematic net name
		PIO0_13/TOUCH_SDA_FC1
I2C_SCL	PIO1_10, PIO0_14	PIO1_10/SE051H_I2C_CLK, PIO0_14/TOUCH_SCL_FC1

2.4 NFC

An NFC reader NXP MFRC630, a high-performance frontend supporting the Read/Write mode for ISO/IEC 14443A, MIFARE, and NTAG products, is connected to the LPC55S69 MCU through an SPI3 interface and two GPIOs. The LPC55S69 can pull up/down one GPIO to enable/disable MFRC630 and receive an interrupt from the other GPIO. The NFC antenna is on the PINPAD board, it is connected to the main board through connector J5. This part is used for touchless access control.

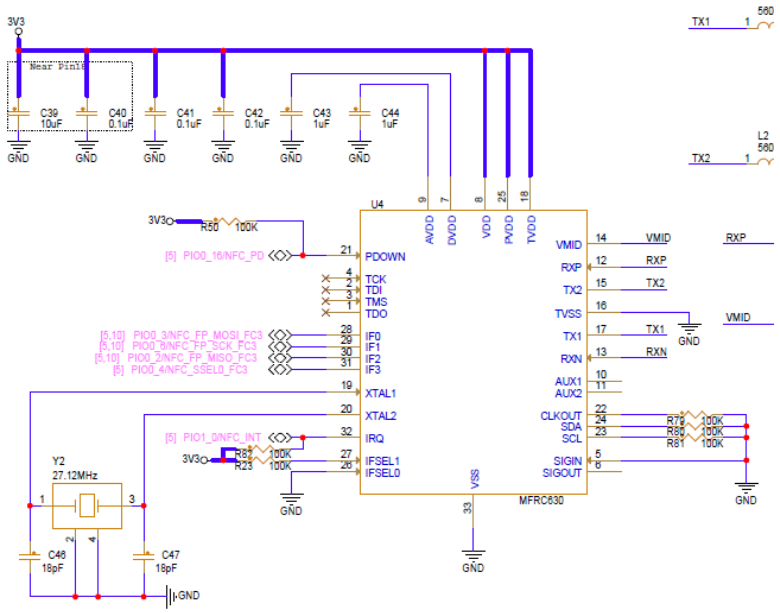


Figure 6. The NFC reader

Table 4. The NFC pin allocation in Smart Access platform

MFRC630 pin	LPC55S69 peripheral (pin)	Schematic net name
PDOWN	PIO0_16/ADC0_8	PIO0_16/NFC_PD
IF0	PIO0_3/TCK	PIO0_3/NFC_FP_MOSI_FC3
IF1	PIO0_6/TDO	PIO0_6/NFC_FP_SCK_FC3
IF2	PIO0_2/TRST	PIO0_2/NFC_FP_MISO_FC3
IF3	PIO0_4/TMS	PIO0_4/NFC_SSEL0_FC3
IRQ	PIO1_0/ADC0_11	PIO1_0/NFC_INT

2.5 Audio

The main board comes pre-assembled with a high-performance, ultra-low-power stereo codec Cirrus Logic WM8904. It converts the audio file stored in the external flash into an analog signal and outputs it to the speaker to realize the voice prompt function. The WM8904 codec is controlled by LPC55S69 MCU through the I2C1 interface, and it receives audio digital signal through the I2S interface. J7 is a connector for the speaker. The schematic of the audio codec WM8904 is shown below.

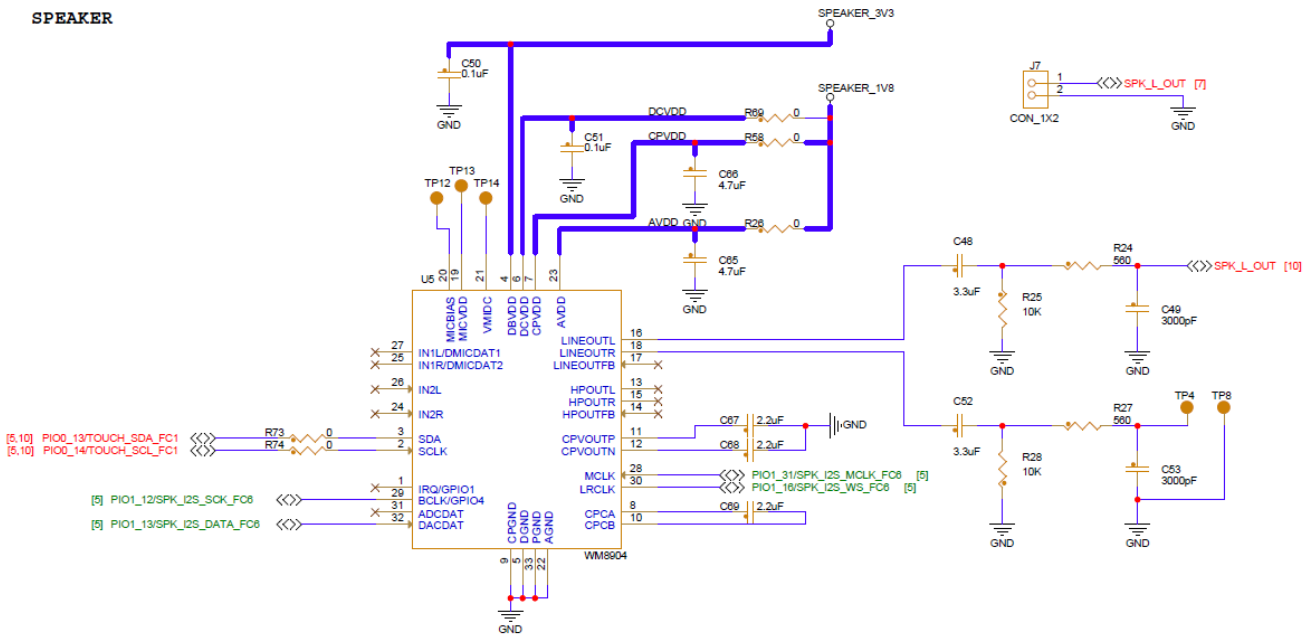


Figure 7. The schematic of audio codec WM8904

Table 5. The audio codec WM8904 pin allocation in Smart Access platform

WM8904 pin	LPC55S69 peripheral (pin)	Schematic net name
SDA	PIO0_13	PIO0_13/TOUCH_SDA_FC1
SCLK	PIO0_14	PIO0_14/TOUCH_SCL_FC1
BCLK/GPIO4	PIO1_12	PIO1_12/SPK_I2S_SCK_FC6
DACDAT	PIO1_13	PIO1_13/SPK_I2S_DATA_FC6
MCLK	PIO1_31	PIO1_31/SPK_I2S_MCLK_FC6
LRCLK	PIO1_16	PIO1_16/SPK_I2S_WS_FC6

2.6 PIR sensor

To meet the low power consumption requirements of some applications such as Smart Lock/Access, a PIR sensor Murata IRA-S210ST01 is embedded on the main board. The PIR signal is amplified, filtered, and translated to a digital signal to be used as an awake up source for the LPC55S69 MCU. The schematic of the PIR sensor is shown below.

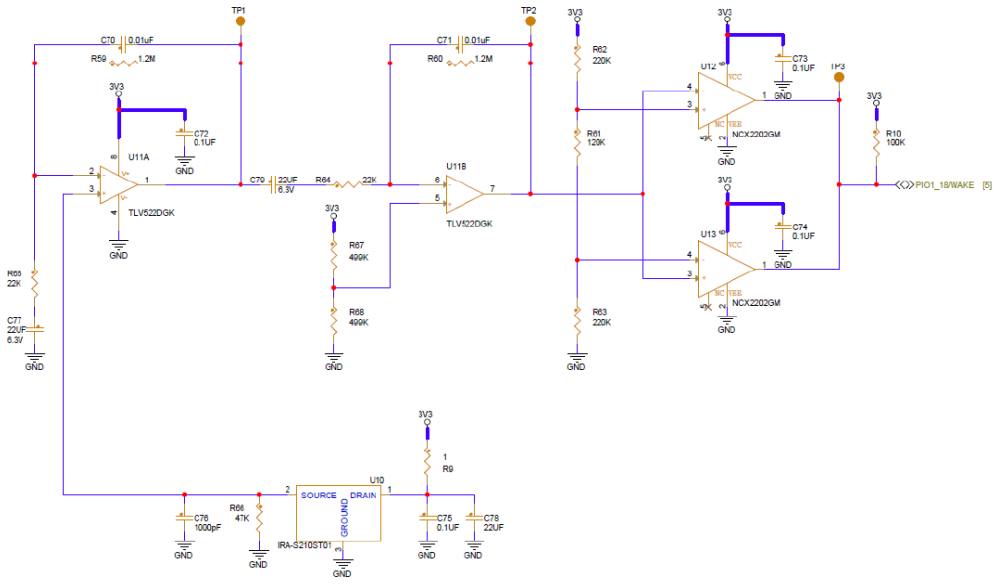


Figure 8. The schematic of the PIR sensor

Table 6. The PIR sensor pin allocation in Smart Access platform

PIR sensor	LPC55S69 peripheral (pin)	Schematic net name
PIR	PIO1_18/WAKUP	PIO1_18/WAKE

2.7 LEDs

The main board embeds 13 LEDs, which are connected to two 8-bit serial-in/serial or parallel-out shift register Nexperia 74HC595PW. These LEDs provide backlighting for the buttons on the touch panel. The LPC55S69 MCU switches the LEDs on and off by sending commands to the 74HC595PW.

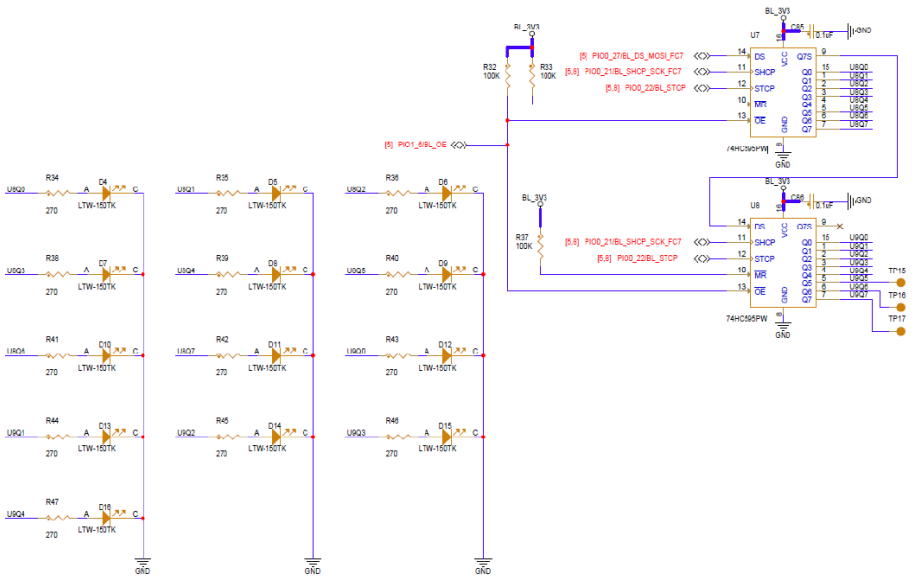


Figure 9. The schematic of LEDs and 74HC595PW

Table 7. The 74HC595PW pin allocation in Smart Access platform

74HC595PW(1)	LPC55S69 peripheral (pin)	Schematic net name
DS	PIO0_27	PIO0_27/BL_DS_MOSI_FC7
SHCP	PIO0_21	PIO0_21/BL_SHCP_SCK_FC7
STCP	PIO0_22	PIO0_22/BL_STCP
OE	PIO1_6	PIO1_6/BL_OE
74HC595PW(2)	**LPC55S69 peripheral (pin)**	**Schematic net name**
DS	-	-
SHCP	PIO0_21	PIO0_21/BL_SHCP_SCK_FC7
STCP	PIO0_22	PIO0_22/BL_STCP
OE	PIO1_6	PIO1_6/BL_OE

2.8 Power circuitry

The main board can be powered from two distinct sources:

- The external connector
- The wireless board connector

Main board can be powered directly by an external power source through connector J1. J4 is a connector for the wireless board. The power supply can be provided by the wireless board. The input range of the power source is 1.8 V-8 V.

There are three LR6232B33M voltage regulators on the main board, one is used to provide 3.3 V to MCU and other components, The remaining two are used to provide 3.3 V and 1.8 V to the WM8904. The PIO0_15 pin of LCP55S69 can control these two LR6232B33M voltage regulators to Enable/Disable.

A 10 megohm resistor and a 5.1 megohm resistor divide the voltage from the wireless board and connect to the ADC pin of the LPC55S69, therefore detecting the magnitude of the input voltage. A P-Channel MOSFET which is controlled by LPC55S69 MCU is used to control the switching of the LEDs.

The schematic of power circuitry is shown below.

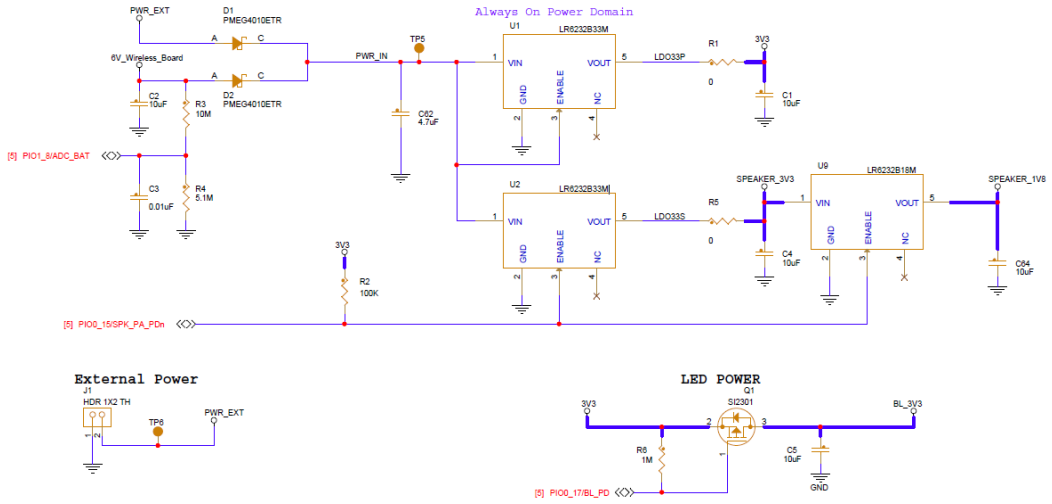


Figure 10. The schematic of power circuitry on the main board

2.9 Connectors

J6 is the 20-pin connector that leads several signal lines, a 3.3 V power source, and GND to the FACECV board. I2C1, UART0, UART5, SPI2, and GPIOs are also included. The I2C1 interface and SPI2 interface are an alternative to the SWM1000SR150 UWB module on the FACECV board. UART0 interface is connected to QN9090 MCU and the UART5 interface is connected to the SLN-VIZN3D-IOT kit.

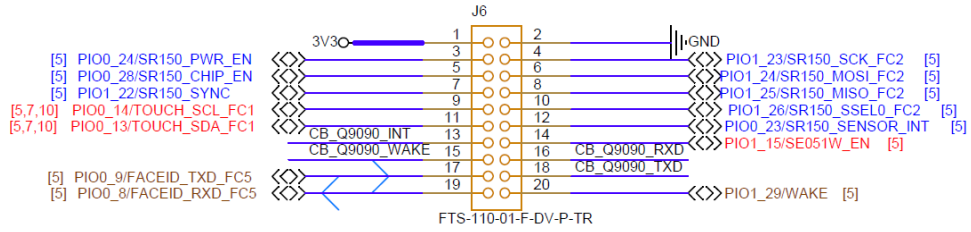


Figure 11. The J6 connector on the main board

Table 8. The J6 connector pin allocation in the main board

J6 connector	LPC55S69 peripheral (pin)	Schematic net name	J6 connector	LPC55S69 peripheral (pin)	Schematic net name
1	-	3V3	2	-	GND
3	PIO0_24	PIO0_24/SR150_PWR_EN	4	PIO1_23	PIO1_23/SR150_SCK_FC2
5	PIO0_28/ WAKEUP	PIO0_28/SR150_CHIP_EN	6	PIO1_24	PIO1_24/SR150_MOSI_FC2
7	PIO1_22	PIO1_22/SR150_SYNC	8	PIO1_25	PIO1_25/SR150_MISO_FC2
9	PIO0_14	PIO0_14/ TOUCH_SCL_FC1	10	PIO1_26	PIO1_26/SR150_SSEL0_FC2

Table continues on the next page...

Table 8. The J6 connector pin allocation in the main board (continued)

J6 connector	LPC55S69 peripheral (pin)	Schematic net name	J6 connector	LPC55S69 peripheral (pin)	Schematic net name
11	PIO0_13	PIO0_13/ TOUCH_SDA_FC1	12	PIO0_23	PIO0_23/ SR150_SENSOR_INT
13	PIO1_5	CB_Q9090_INT	14	PIO1_15	PIO1_15/SE051W_EN
15	PIO0_31/ADC0_3	CB_Q9090_WAKE	16	PIO0_29	CB_Q9090_RXD
17	PIO0_9/ACMP0_B	PIO0_9/FACEID_TXD_FC5	18	PIO0_30	CB_Q9090_TXD
19	PIO0_8	PIO0_8/ FACEID_RXD_FC5	20	PIO1_29	PIO1_29/WAKE

J5 is a 10-pin connector for the PINPAD board. One I2C interface and two GPIOs of the LPC55S69 are connected to the KL16 MCU on the PINPAD board. The two NFC signals are connected to the antenna on the PINPAD board.

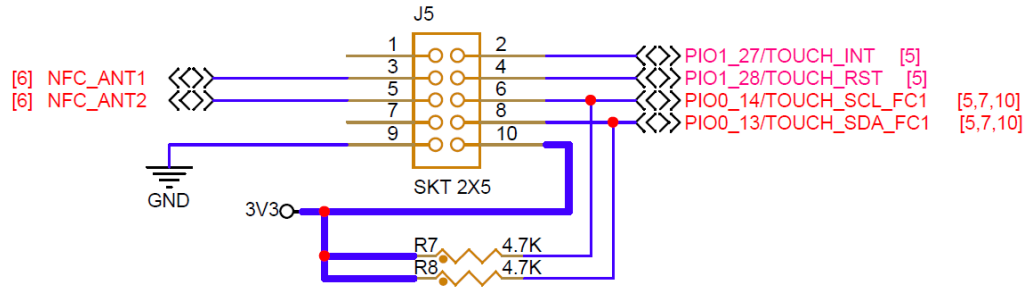


Figure 12. The J5 connector on the main board

Table 9. The J5 connector pin allocation in the main board

J5 connector	LPC55S69 peripheral (pin)	Schematic net name	J5 connector	LPC55S69 peripheral (pin)	Schematic net name
1	NC	NC	2	PIO1_27	PIO1_27/TOUCH_INT
3	-	NFC_ANT1	4	PIO1_28	PIO1_28/TOUCH_RST
5	-	NFC_ANT2	6	PIO0_14	PIO0_14/TOUCH_SCL_FC1
7	NC	NC	8	PIO0_13	PIO0_13/TOUCH_SDA_FC1
9	-	GND	10	-	3V3

J6 is the 20-pin connector that is connected to the wireless board, it receives a 6 V power supply from the wireless board to power the entire main board. Two PWM signals, two UART interfaces, and several GPIOs are connected to the wireless board to control the motor and communicate with the QN9090 module and K32W061 module.

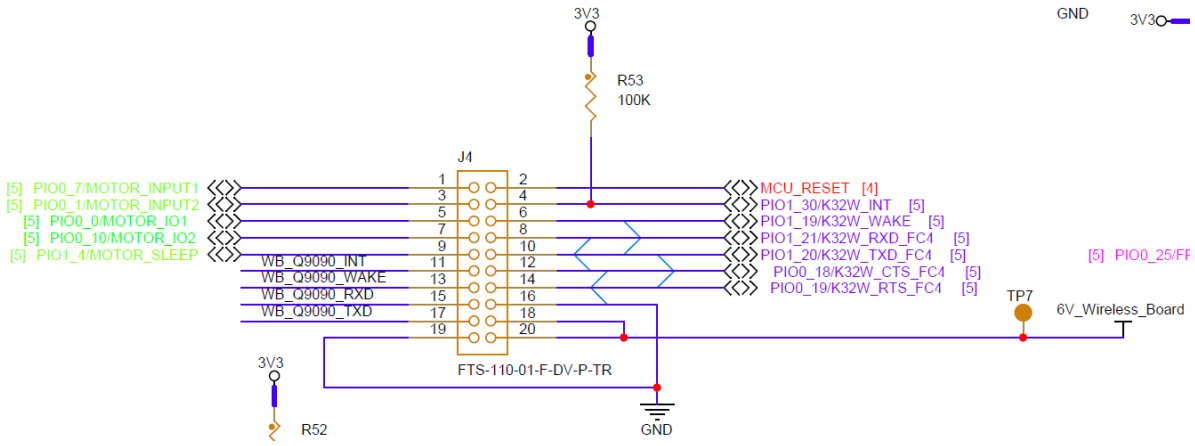


Figure 13. The J4 connector on the main board

Table 10. The J4 connector pin allocation in the main board

J4 connector	LPC55S69 peripheral (pin)	Schematic net name	J4 connector	LPC55S69 peripheral (pin)	Schematic net name
1	PIO0_7	PIO0_7/ MOTOR_INPUT1	2	-	MCU_RESET
3	PIO0_1	PIO0_1/ MOTOR_INPUT2	4	PIO1_30	PIO1_30/K32W_INT
5	PIO0_0	PIO0_0/MOTOR_IO1	6	PIO1_19	PIO1_19/K32W_WAKE
7	PIO0_10	PIO0_10/MOTOR_IO2	8	PIO1_21	PIO1_21/ K32W_RXD_FC4
9	PIO1_4	PIO1_4/ MOTOR_SLEEP	10	PIO1_20	PIO1_20/ K32W_TXD_FC4
11	PIO1_5	WB_Q9090_INT	12	PIO0_18	PIO0_18/ K32W_CTS_FC4
13	PIO0_31	WB_Q9090_WAKE	14	PIO0_19	PIO0_19/ K32W_RTS_FC4
15	PIO0_29	WB_Q9090_RXD	16	GND	GND
17	PIO0_30	WB_Q9090_TXD	18	-	6 V
19	GND	GND	20	-	6 V

J3 is the 8-pin connector for the fingerprint module, it supplies a 3.3 V power source to the fingerprint module and set up communication through the SPI3 interface.

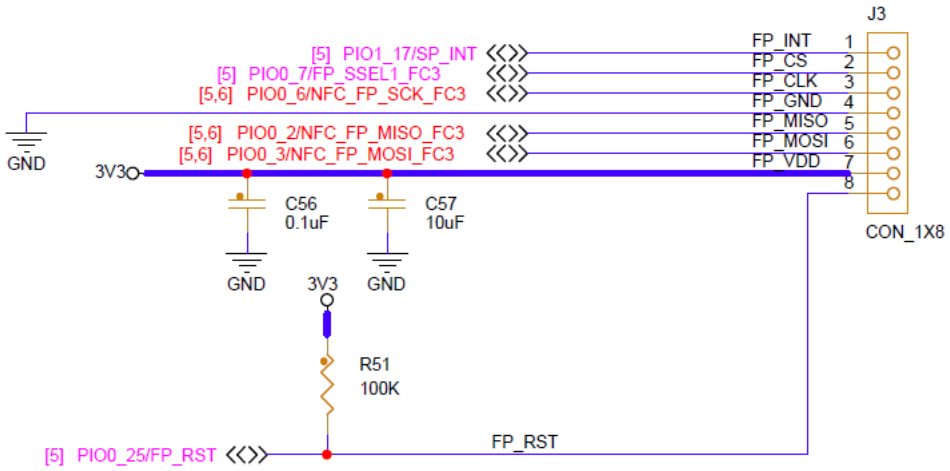


Figure 14. The J3 connector on the main board

Table 11. The J3 connector pin allocation in the main board

J3 connector	LPC55S69 peripheral (pin)	Schematic net name	J3 connector	LPC55S69 peripheral (pin)	Schematic net name
1	PIO1_17	PIO1_17/SP_INT	2	PIO0_7	PIO0_7/FP_SSEL1_FC3
3	PIO0_6	PIO0_6/NFC_FP_SCK_FC3	4	-	GND
5	PIO0_2	PIO0_2/ NFC_FP_MISO_FC3	6	PIO0_3	PIO0_3/ NFC_FP_MOSI_FC3
7	-	3V3	8	PIO0_25	PIO0_25/FP_RST

Chapter 3
Wireless board

This chapter provides detailed information about the electrical design and practical considerations of the wireless board. The wireless board supports Matter control. IEEE 802.15.4 mesh network protocols, Zigbee, and Thread as well as Bluetooth Low Energy 5.0. The pictures of the wireless board are shown below.

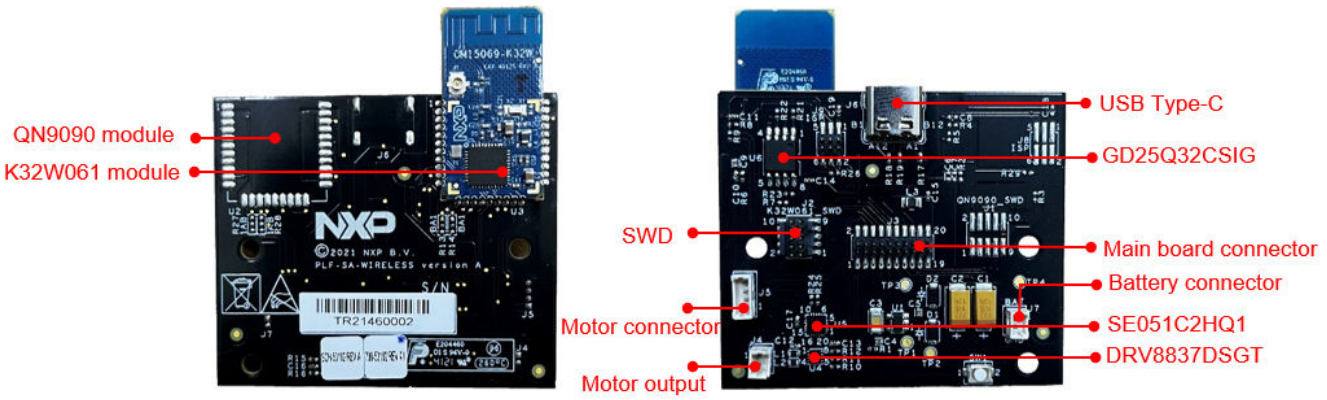


Figure 15. The wireless board callout

3.1 Wireless connectivity

3.1.1 OM15069 K32W module (default)

The K32W061 is ultra-low power, high-performance Arm® Cortex®-M4-based wireless microcontrollers supporting Zigbee 3.0, Thread, and Bluetooth Low Energy 5.0 networking stacks to facilitate smart access/lock applications.

The K32W061 includes a 2.4 GHz Bluetooth Low Energy 5 (supporting eight simultaneous connections) compliant transceiver, a 2.4 GHz IEEE 802.15.4 compliant transceiver, and a comprehensive mix of analog and digital peripherals.

Ultra-low current consumption in both radio receive and transmit modes and also in the power-down modes allow the use of coin cell batteries.

The K32W061 has 640 kB embedded Flash, 152 kB RAM, and 128 kB ROM memory. The embedded flash can support Over The Air (OTA) code download to applications. The devices also include a 10-channel PWM, two timers, one RTC/alarm timer, a Windowed Watchdog Timer (WWDT), two USARTs, two SPI interfaces, two I2C interfaces, a DMIC subsystem consisting of a dual-channel PDM microphone interface with voice activity detector, one 12-bit ADC, temperature sensor, and a comparator.

The schematic of the OM15069-K32W module is shown below.

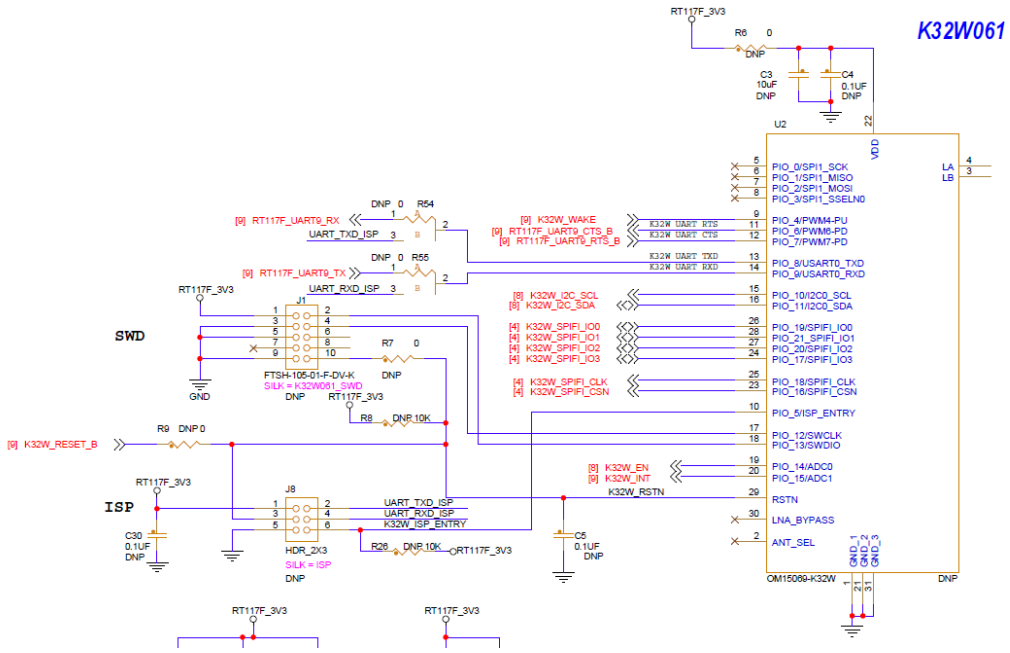


Figure 16. OM15069-K32W module

A pushbutton is connected to the RSTIN pin (reset input) of the OM15069-K32W module.

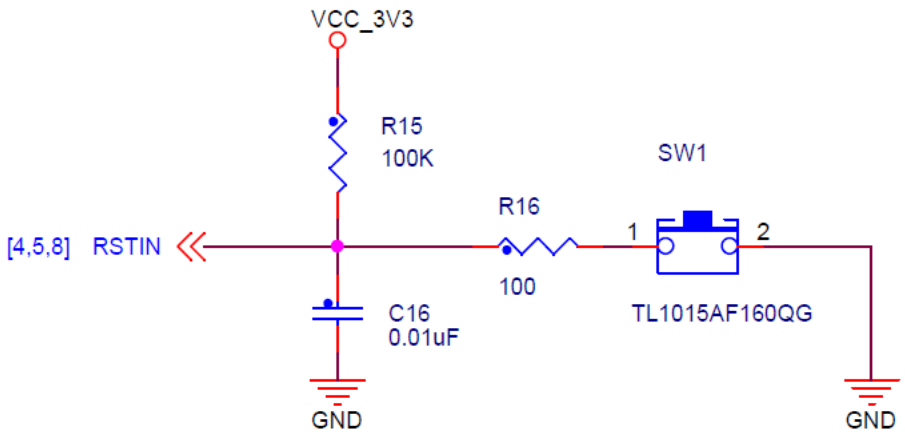


Figure 17. The reset button of OM15069-K32W module

3.1.2 OM15069-2 module (option)

The wireless board integrates an NXP OM15069-2 module, which is an independent system board with a QN9090 SoC. The QN9090 SoC integrates a radio transceiver operating in the 2.4 GHz ISM band supporting BLE Radio, an Arm Cortex-M4 processor, up to 640 kB flash, 152 kB SRAM, and 128 kB ROM. The module also integrates BLE Link layer processing hardware and peripherals optimized to meet the requirements of the target applications.

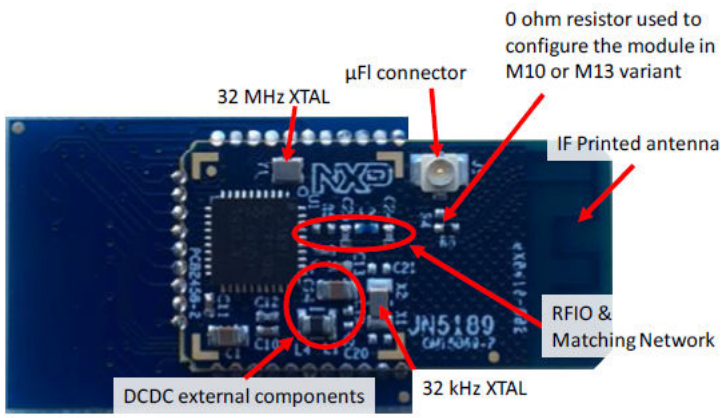
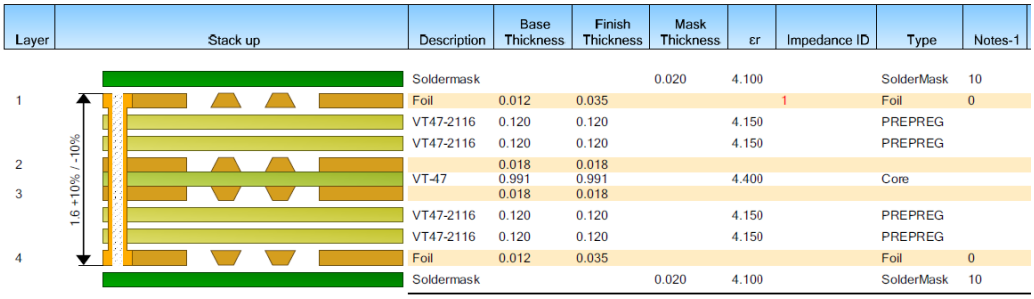


Figure 18. OM15069-2 module

The OM15069-2 module is built on a standard 4-layer printed circuit board (PCB) with the individual layers organized as shown below.



Layer	Stack up	Description	Base Thickness	Finish Thickness	Mask Thickness	εr	Impedance ID	Type	Notes-1
		Soldermask			0.020	4.100		SolderMask	10
1		Foil	0.012	0.035			1	Foil	0
		VT47-2116	0.120	0.120		4.150		PREPREG	
		VT47-2116	0.120	0.120		4.150		PREPREG	
2			0.018	0.018					
		VT-47	0.991	0.991		4.400		Core	
3			0.018	0.018					
		VT47-2116	0.120	0.120		4.150		PREPREG	
		VT47-2116	0.120	0.120		4.150		PREPREG	
4		Foil	0.012	0.035				Foil	0
		Soldermask			0.020	4.100		SolderMask	10

1.6 +10% / -10%

Figure 19. OM15069-2 stack-up information

The OM15069-2 module is soldered on the wireless board and transmits data to the LPC55S69 on the main board through the UART interface. The module routes two GPIOs: one for generating an interrupt to LPC55S6, the other for receiving the wake-up signal from the LPC55S69. The SWD interface is also routed to a 10-pin standard header for reprogramming and Firmware debugging. The schematic for the OM15069-2 module is shown below.

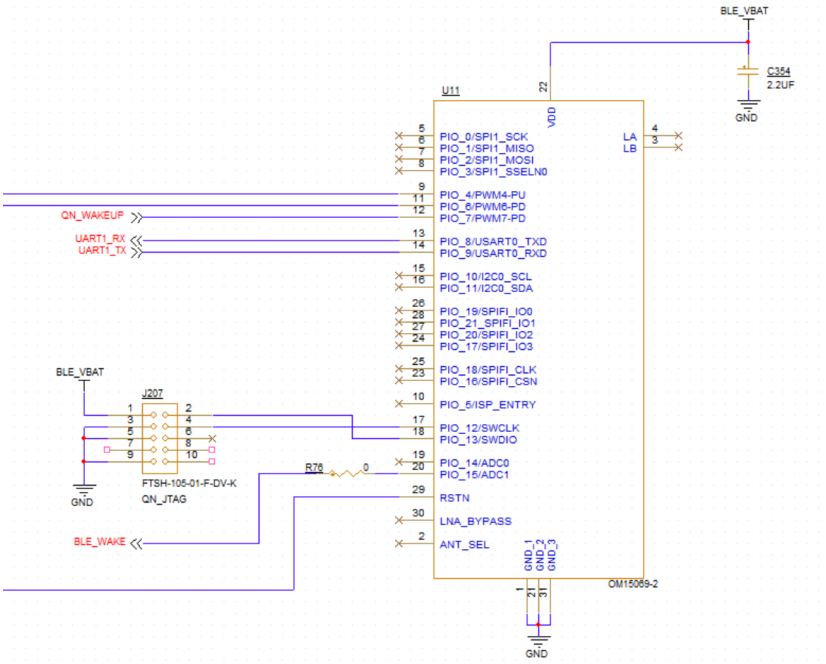


Figure 20. Bluetooth OM15069-2 module

Table 12. OM15069-2 module pin allocation in the wireless board

OM15069-2 module	LPC55S69 Peripheral (Pin)	Schematic Net Name
PIO_8/USART0_TXD	PIO0_30	QN9090_UART_TX
PIO_9/USART0_RXD	PIO0_29	QN9090_UART_RX
PIO_7/PWM7-PD	PIO0_31	QN9090_WAKE
PIO_15/ADC1	PIO1_5	QN9090_INT

3.2 Memories

One 32 Mbit/4 MB serial Quad SPI NOR flash memory GigaDevice GD25Q32C is connected to the K32W061 MCU through its SPIFI interface in Quad SPI mode. This external memory stores the K32W061 application, which boots after reset, power cycle, or wake-up.

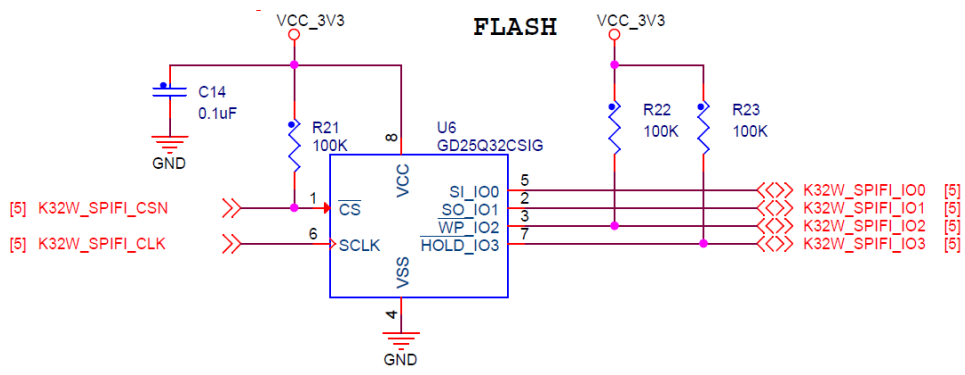


Figure 21. GD25Q32C Quad SPI NOR flash

Table 13. GD25Q32C pin allocation in the wireless board

GD25Q32C pin	K32W061 peripheral (pin)	Schematic net name
CS	PIO_16/SPIFI_CSN	K32W_SPIFI_CSN
SCLK	PIO_18/SPIFI_CLK	K32W_SPIFI_CLK
SI_IO0	PIO_19/SPIFI_IO0	K32W_SPIFI_IO0
SO_IO1	PIO_21_SPIFI_IO1	K32W_SPIFI_IO1
WP_IO2	PIO_20/SPIFI_IO2	K32W_SPIFI_IO2
HOLD_IO3	PIO_17/SPIFI_IO3	K32W_SPIFI_IO3

3.3 Security

The wireless board embeds an NXP SE051H security element, which supports applet updates in the field and delivers proven security certified to CC EAL 6+, with AVA_VAN.5 up to the OS level. It is connected to the K32W061 MCU through I2C interface, as well as a GPIO for Enable/Disable. It provides security protection for K32W061.

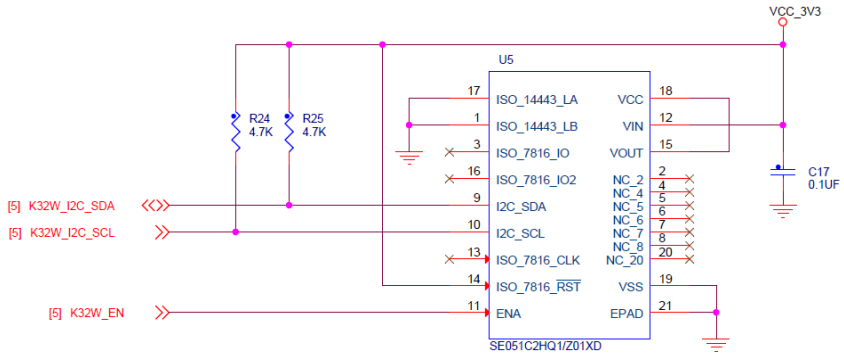


Figure 22. SE051H security element on the wireless board

Table 14. SE051H pin allocation in Smart Access platform

SE051H pin	K32W061 peripheral (pin)	Schematic net name
I2C_SDA	PIO_11/I2C0_SDA	K32W_I2C_SDA
I2C_SCL	PIO_10/I2C0_SCL	K32W_I2C_SCL
ENA	PIO_14/ADC0	K32W_EN

3.4 Motor driver

A 1.8 A low voltage brushed DC motor driver DRV8837DSGT (PWM Ctrl) is embedded on the wireless board. Its output driver block consists of N-channel power MOSFETs configured as an H-bridge to drive the motor winding to control the door lock. Two input pins are connected to LPC55S69 which can provide PWM signals through the J3 connector. Two output pins are connected to a DC motor through the J4 connector. An additional GPIO from LPC55S69 is used to control sleep mode of motor driver DRV8837DSGT.

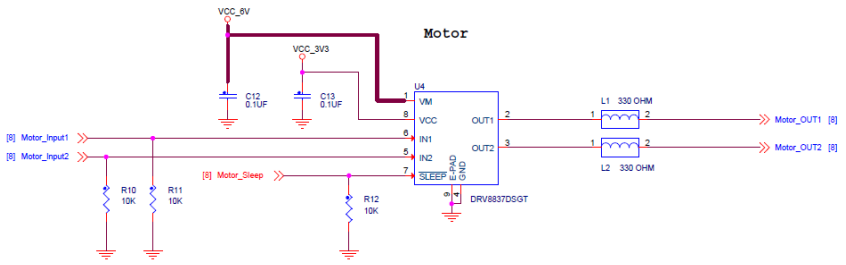


Figure 23. Brushed DC motor driver DRV8837DSGT on the wireless board

Table 15. DRV8837DSGT pin allocation in the wireless board

DRV8837DSGT pin	J3 connector (pin)	J4 connector (pin)	Schematic net name
IN1	Pin 1	-	Motor_Input1
IN2	Pin 3	-	Motor_Input2
OUT1	-	Pin 1	Motor_OUT1
OUT2	-	Pin 2	Motor_OUT2
SLEEP	Pin 9	-	Motor_Sleep

3.5 Power circuitry

The wireless board can be powered from two distinct sources:

- The USB type-C
- The battery connector

The Wireless board can be powered through a J6 USB type-C connector. J7 can be connected to a battery box that can hold 4x1.5 V batteries. Whatever power supply input is selected, it is connected to a voltage regulator LR6232B33M to provide the 3.3 V.

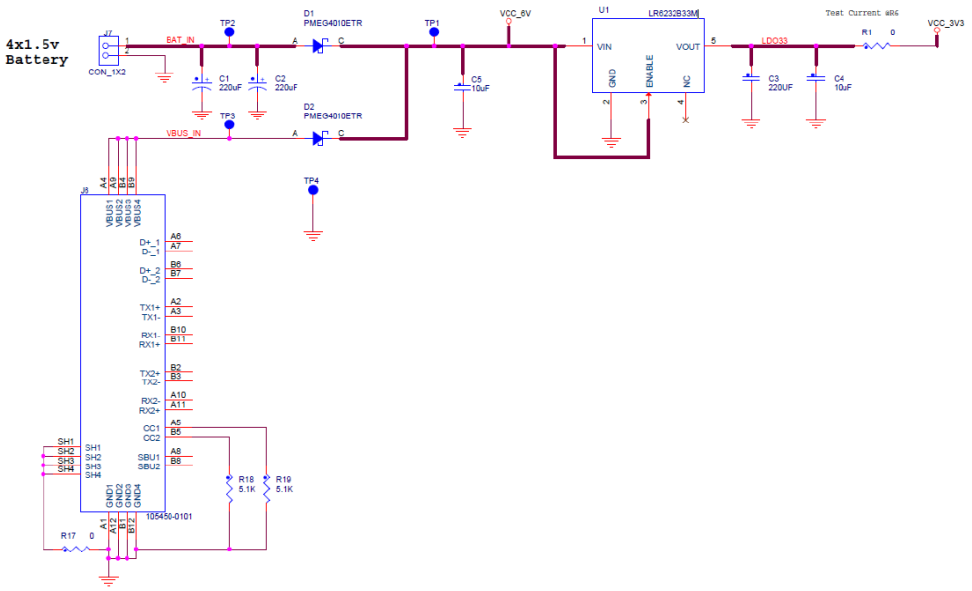


Figure 24. Power circuitry on the wireless board

3.6 Connectors

J3 is the 20-pin connector which leads several signal lines, 6 V power source, and GND to the main board. OM15069 K32W module and OM15069-2 module are connected and controlled by LPC55S69 through J3 connector.

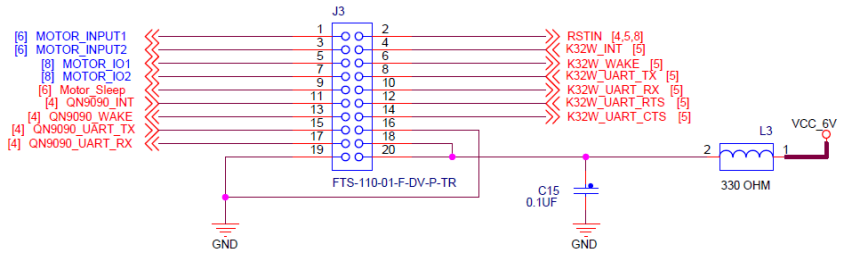


Figure 25. J3 connector on the wireless board

Table 16. The J3 connector pin allocation in the wireless board

J3 connector	Pins of components	Schematic net name	J3 connector	Pins of components	Schematic net name
1	DRV8837DSGT-IN1	MOTOR_INPUT1	2	OM15069-K32W RSTN	RSTIN
3	DRV8837DSGT-IN2	MOTOR_INPUT2	4	OM15069-K32W- K32W_INT	K32W_INT
5	J5-Pin 2	MOTOR_IO1	6	OM15069-K32W- K32W_WAKE	K32W_WAKE

Table continues on the next page...

Table 16. The J3 connector pin allocation in the wireless board (continued)

J3 connector	Pins of components	Schematic net name	J3 connector	Pins of components	Schematic net name
7	J5-Pin 3	MOTOR_IO2	8	OM15069-K32W-PIO_8/USART0_TXD	K32W_UART_TX
9	DRV8837DSGT-SLEEP	Motor_Sleep	10	OM15069-K32W-PIO_9/USART0_RXD	K32W_UART_RX
11	OM15069-2-PIO_15/ADC1	QN9090_INT	12	OM15069-K32W-PIO_6/PWM6-PD	K32W_UART_RTS
13	OM15069-2-PIO_7/PWM7-PD	QN9090_WAKE	14	OM15069-K32W-PIO_7/PWM7-PD	K32W_UART_CTS
15	OM15069-2-PIO_8/USART0_TXD	QN9090_UART_TX	16	GND	GND
17	OM15069-2- PIO_9/ USART0_RXD	QN9090_UART_RX	18	VCC_6V	VCC_6V
19	GND	GND	20	VCC_6V	VCC_6V

Chapter 4
PINPAD board

This chapter provides detailed information about the electrical design and practical considerations of the PINPAD board. The PINPAD board has 13 touch pads and an NFC antenna. It is used for pin pad and NFC access control. The PINPAD board pictures are shown below.

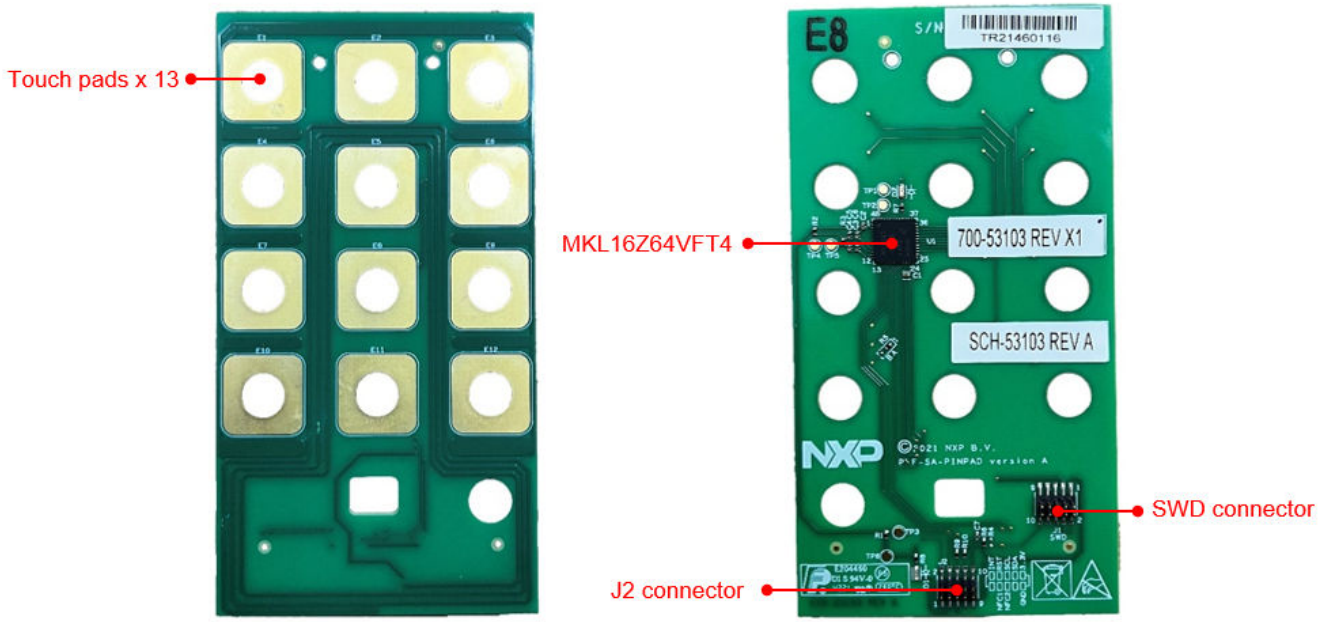


Figure 26. The PINPAD board callout

4.1 MKL16Z64VFT4 microcontroller

MKL16Z64VFT4 is an ultra-low-power 32-bit microcontroller, it provides a low-power hardware touch sensor interface to control 13 touch pads and communicates with LPC55S69 MCU through an I2C interface. The schematic of the MKL16Z64VFT4 microcontroller is shown below.

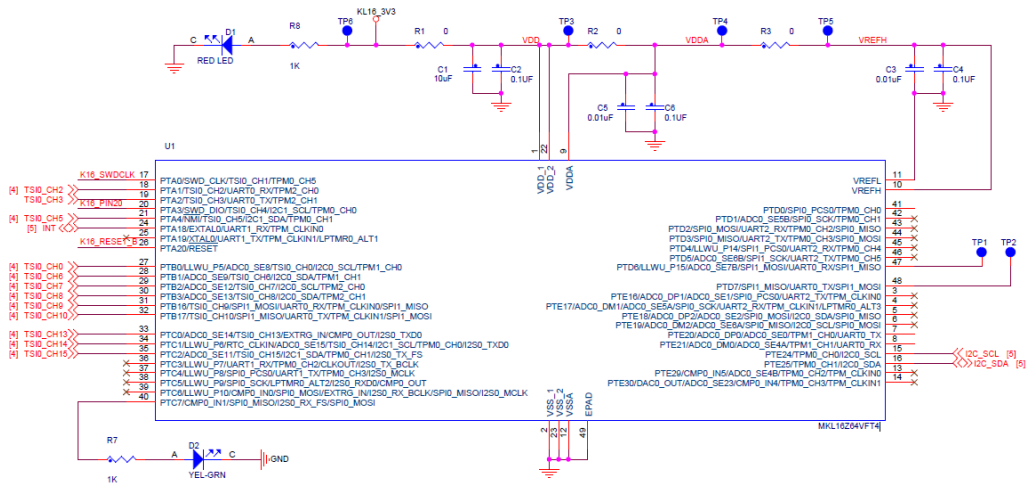


Figure 27. The schematic of MKL16Z64VFT4 microcontroller

4.2 Touch pads

13 touch pads are integrated on the PINPAD board. Each of them consists of a copper block and connects to a low-power hardware touch sensor interface of MKL16Z64VFT4. One of the touch pads is used for special controls such as the wake-up of the system.

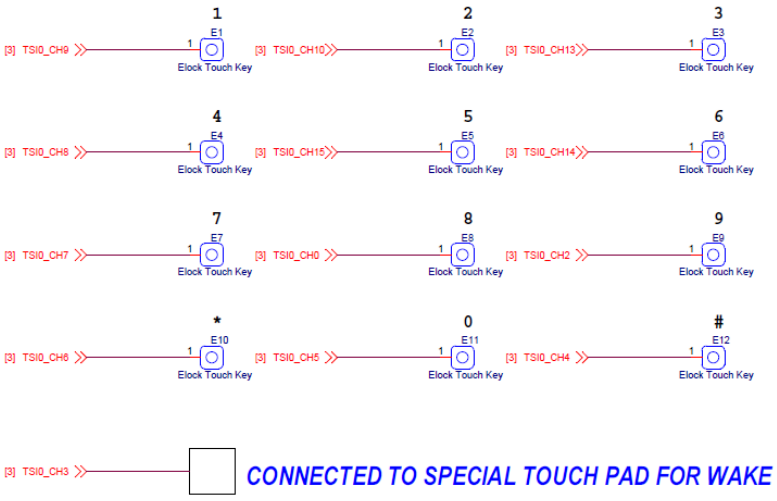


Figure 28. The schematic of touch pads

Table 17. Touch pads pin allocation in Smart Access platform

Touch pads pin	MKL16Z64VFT4 peripheral (pin)	Schematic net name	Touch pads Pin	MKL16Z64VFT4 peripheral (pin)	Schematic net name
E1	PTB16	TSI0_CH9	E2	PTB17	TSI0_CH10
E3	PTC0	TSI0_CH13	E4	PTB3	TSI0_CH8

Table continues on the next page...

Table 17. Touch pads pin allocation in Smart Access platform (continued)

Touch pads pin	MKL16Z64VFT4 peripheral (pin)	Schematic net name	Touch pads Pin	MKL16Z64VFT4 peripheral (pin)	Schematic net name
E5	PTC2	TSI0_CH15	E6	PTC1	TSI0_CH14
E7	PTB2	TSI0_CH7	E8	PTB0	TSI0_CH0
E9	PTA1	TSI0_CH2	E10	PTB1	TSI0_CH6
E11	PTA4	TSI0_CH5	E12	PTA3	TSI0_CH4
E13	PTA2	TSI0_CH3	-	-	-

4.3 NFC antenna

The NFC antenna is integrated into the PINPAD board for short-distance transmission. It is connected to the NFC reader MFRC630 on the main board through the J2 connector.

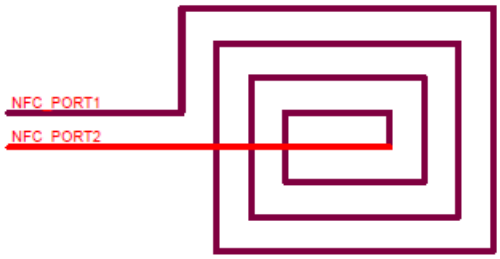


Figure 29. The schematic of NFC antenna

Table 18. NFC antenna pin allocation in Smart Access platform

NFC antenna pin	J2 connector (pin)	Schematic net name
1	PIN-3	NFC_PORT1
2	PIN-5	NFC_PORT2

4.4 Connectors

There are two connectors on the PINPAD board. J1 is used for debugging while J2 connects to the main board. The schematic of the J1 connector is shown below, J1 connector is connected to the SWD interface of MKL16Z64VFT4.

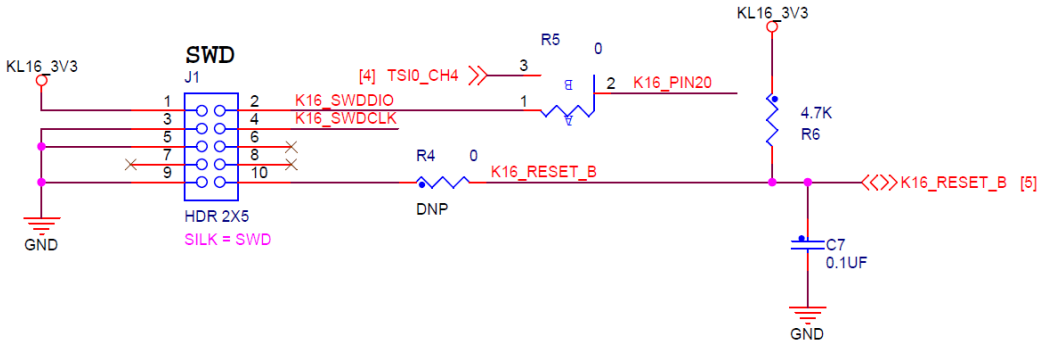


Figure 30. J1 connector on the PINPAD board

Table 19. J1 connector pin allocation in the PINPAD board

J1 connector pin	MKL16Z64VFT4 peripheral (pin)	Schematic net name	J1 connector pin	MKL16Z64VFT4 peripheral (pin)	Schematic net name
1	KL16_3V3	KL16_3V3	2	PTA3	K16_SWDDIO
3	GND	GND	4	PTA0	K16_SWDCLK
5	GND	GND	6	-	-
7	-	-	8	-	-
9	GND	GND	10	PTA20	K16_RESET_B

The J2 connector is connected to the main board, including I2C signal, NFC antenna, and so on.

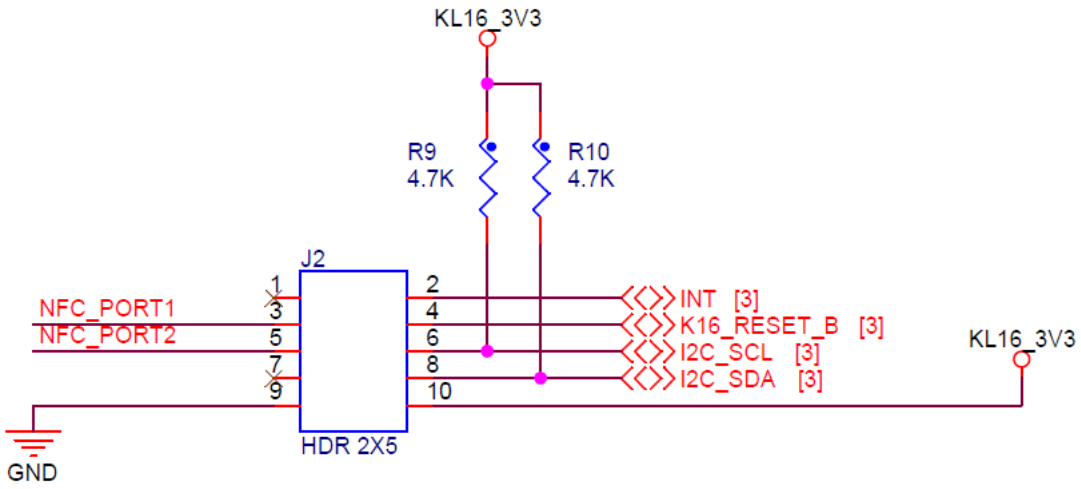


Figure 31. J2 connector on the PINPAD board

Table 20. J2 connector pin allocation in the PINPAD board

J2 connector pin	MKL16Z64VFT4 peripheral (pin)	Schematic net name	J2 connector pin	MKL16Z64VFT4 peripheral (pin)	Schematic net name
1	-	-	2	PTA18	INT
3	NFC_PORT1	NFC_PORT1	4	PTA20	K16_RESET_B
5	NFC_PORT2	NFC_PORT2	6	PTE24	I2C_SCL
7	-	-	8	PTE25	I2C_SDA
9	GND	GND	10	KL16_3V3	KL16_3V3

Chapter 5
FaceCV board

The FaceCV board is a conversion board for the SLN-VIZN3D-IOT kit. It does not only connect the main board and SLN-VIZN3D-IOT kit but also provides wireless control options, including Matter control and UWB control. An OM15069-K32W module, a QN9090 MCU, and an SWM1000SR150 module are embedded on this board. The pictures of the VIZN3D conversion board are shown below.

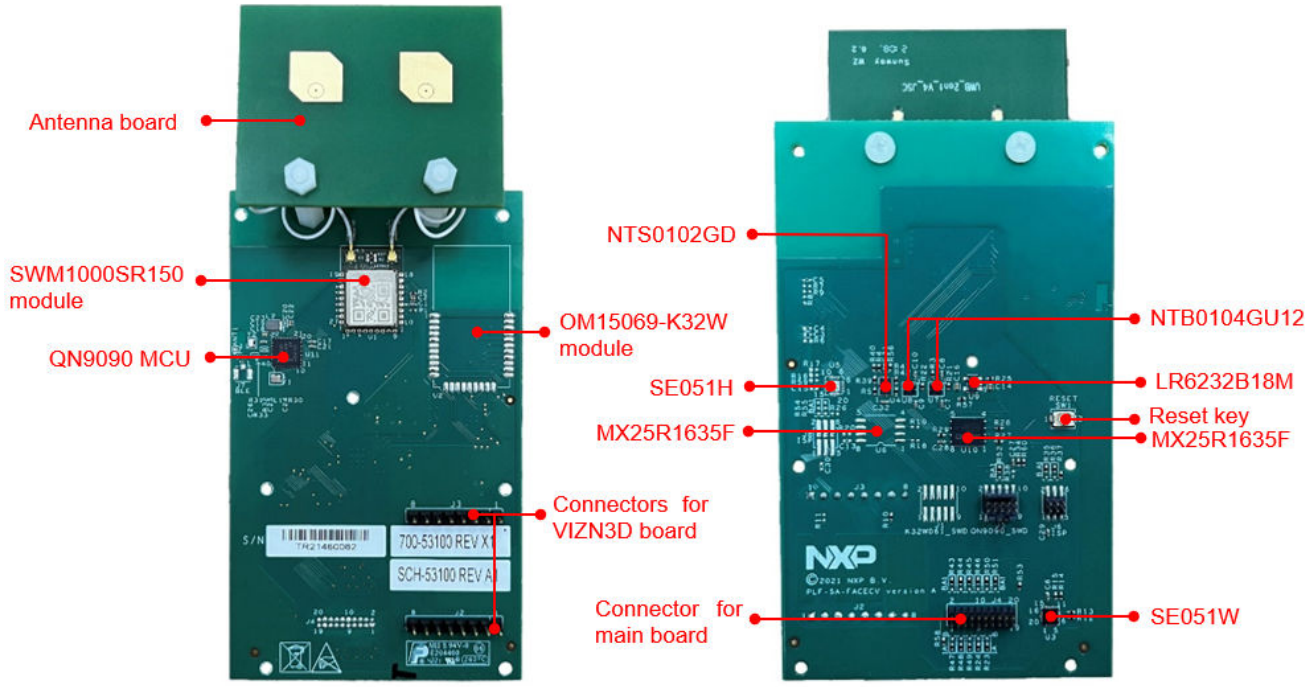


Figure 32. The VIZN3D conversion board callout

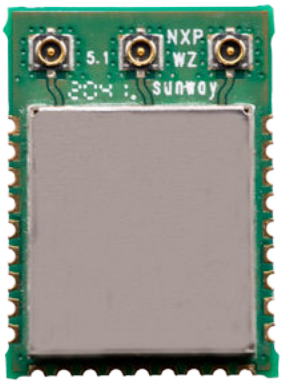
5.1 Wireless connectivity

5.1.1 SWM1000SR150 module

Based on the NXP chip, the SWM1000SR150 UWB module integrates the clock circuit, RF circuit, power management, and so on, which conforms to the IEEE 802.15.4z HRP UWB standard. PHY and MAC conform to the FiRa Consortium specification.

SWM1000SR150 module can be used for single-side two ways ranging (TWR) or double-side two-ways ranging using an External Antennas (designed by Sunway). It can also be used for the 2D/3D real-time location system (RTLS).

Table 21. Key features of SWM1000SR150 module



Name	SWM1000SR150
Antenna type	JSC
Size	13 mm * 18 mm * 2.2 mm
Communication interface	SPI
Main chip	SR150
channel	5 and 9
Frequency range	6.24 GHz~8.24 GHz
Supply voltage	2.2 V ~ 5.5 V(with DC-DC) 1.71 V ~ 1.98 V(without DC-DC)
Max output power	11.5 dBm
Ranging mode	1D/2D/3D Ranging

The SWM1000SR150 module can be connected to LPC55S69 MCU on the main board through the J4 connector or be connected to QN9090 MCU on the FACECV board. Due to the difference in supply voltage between LPC55S69/QN9090 MCU and SWM1000SR150 module, three dual supply-translating transceivers with auto direction sensing are used, including two NTB0104GU12 transceivers and an NTS0102GD transceiver.

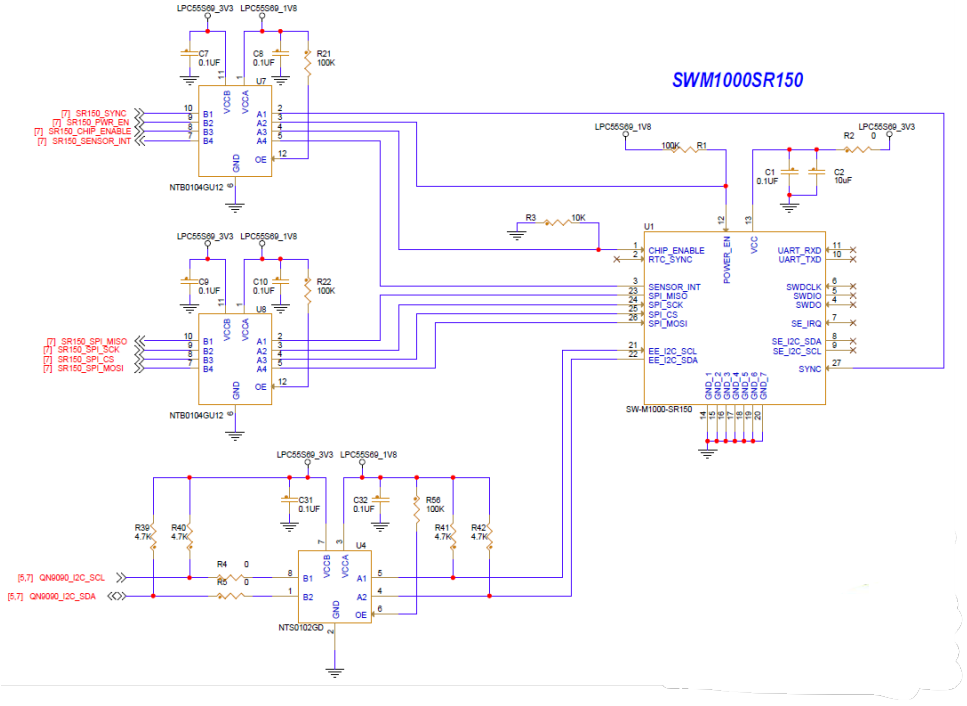


Figure 33. The schematic of SWM1000SR150 module on the FACECV board

Table 22. The SWM1000SR150 module pin allocation in the FACECV board

J4 connector	QN9090 MCU	SWM1000SR150 (pin)	Schematic net name
LPC55_SR150_SYNC	QN9090_SR_SYNC	SYNC	SR150_SYNC
LPC55_SR150_PWR_EN	QN9090_SR_PWREN	POWER_EN	SR150_PWR_EN
LPC55_SR150_CHIP_EN	QN9090_SR_CHIPEN	CHIP_ENABLE	SR150_CHIP_ENABLE
LPC55_SR150_SENSOR_INT	QN9090_SR_SSRINT	SENSOR_INT	SR150_SENSOR_INT
LPC55_SPI_MISO	QN9090_SR_MISO	SPI_MISO	SR150_SPI_MISO
LPC55_SPI_SCK	QN9090_SR_SCK	SPI_SCK	SR150_SPI_SCK
LPC55_SPI_CS	QN9090_SR_CS	SPI_CS	SR150_SPI_CS
LPC55_SPI_MOSI	QN9090_SR_MOSI	SPI_MOSI	SR150_SPI_MOSI
-	QN9090_I2C_SCL	EE_I2C_SCL	QN9090_I2C_SCL
-	QN9090_I2C_SDA	EE_I2C_SDA	QN9090_I2C_SDA

5.1.2 OM15069 K32W module

The K32W061 is ultra-low power, high-performance Arm® Cortex®-M4-based wireless microcontrollers supporting Zigbee 3.0, Thread, and Bluetooth Low Energy 5.0 networking stacks to facilitate smart access/lock applications.

The K32W061 includes a 2.4 GHz Bluetooth Low Energy 5 (supporting eight simultaneous connections) compliant transceiver, a 2.4 GHz IEEE 802.15.4 compliant transceiver, and a comprehensive mix of analog and digital peripherals.

Ultra-low current consumption in both radio receive and transmit modes and also in the power-down modes allow the use of coin cell batteries.

The K32W061 has 640 kB embedded Flash, 152 kB RAM, and 128 kB ROM memory. The embedded flash can support Over The Air (OTA) code download to applications. The devices also include a 10-channel PWM, two timers, one RTC/alarm timer, a Windowed Watchdog Timer (WWDT), two USARTs, two SPI interfaces, two I2C interfaces, a DMIC subsystem consisting of a dual-channel PDM microphone interface with voice activity detector, one 12-bit ADC, temperature sensor and a comparator.

It is connected to the VIZN3D kit through a UART interface. The schematic of the OM15069-K32W module is shown below.

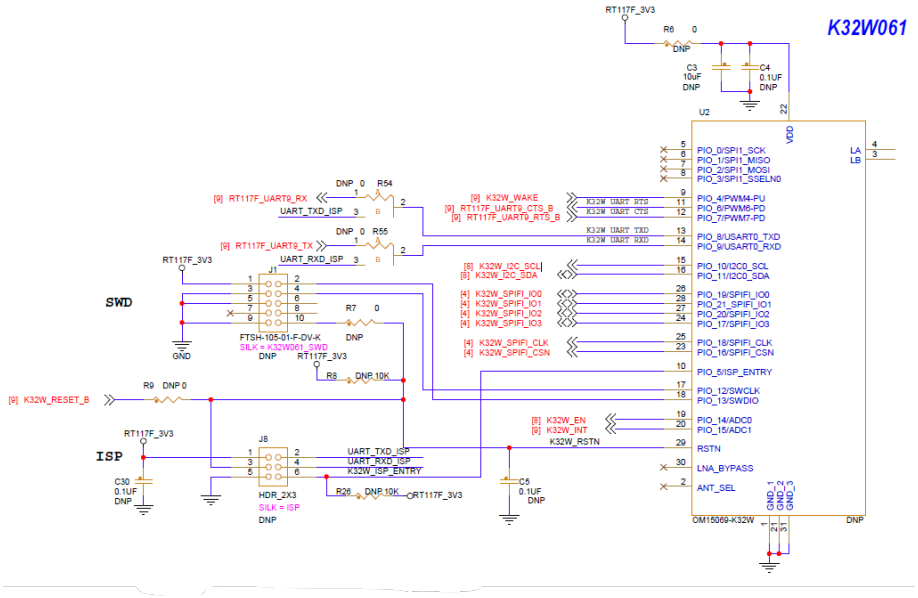


Figure 34. The schematic of OM15069 K32W module on the FACECV board

Table 23. The OM15069 K32W module pin allocation in the FACECV board

OM15069 K32W module	J2 andJ3 connector (pin)	Schematic net name
PIO_8/USART0_TXD	J2-Pin 3	RT117F_UART9_RX
PIO_9/USART0_RXD	J2-Pin 4	RT117F_UART9_TX
PIO_15/ADC1	J2-Pin 1	K32W_INT
RSTN	J2-Pin 2	K32W_RESET_B
PIO_4/PWM4-PU	J3-Pin 1	K32W_WAKE
PIO_6/PWM6-PD	J2-Pin 6	RT117F_UART9_CTS_B
PIO_7/PWM7-PD	J2-Pin 5	RT117F_UART9_RTS_B

5.1.3 QN9090 MCU

The QN9090 SoC integrates a radio transceiver operating in the 2.4 GHz ISM band supporting BLE Radio, an Arm Cortex-M4 processor, up to 640 kB flash, 152 kB SRAM, and 128 kB ROM. It can control the SWM1000SR150 UWB module, an external flash MX25R1635F, and a security element SE051W. It can be woken up by LPC55S69 and send an interrupt signal.

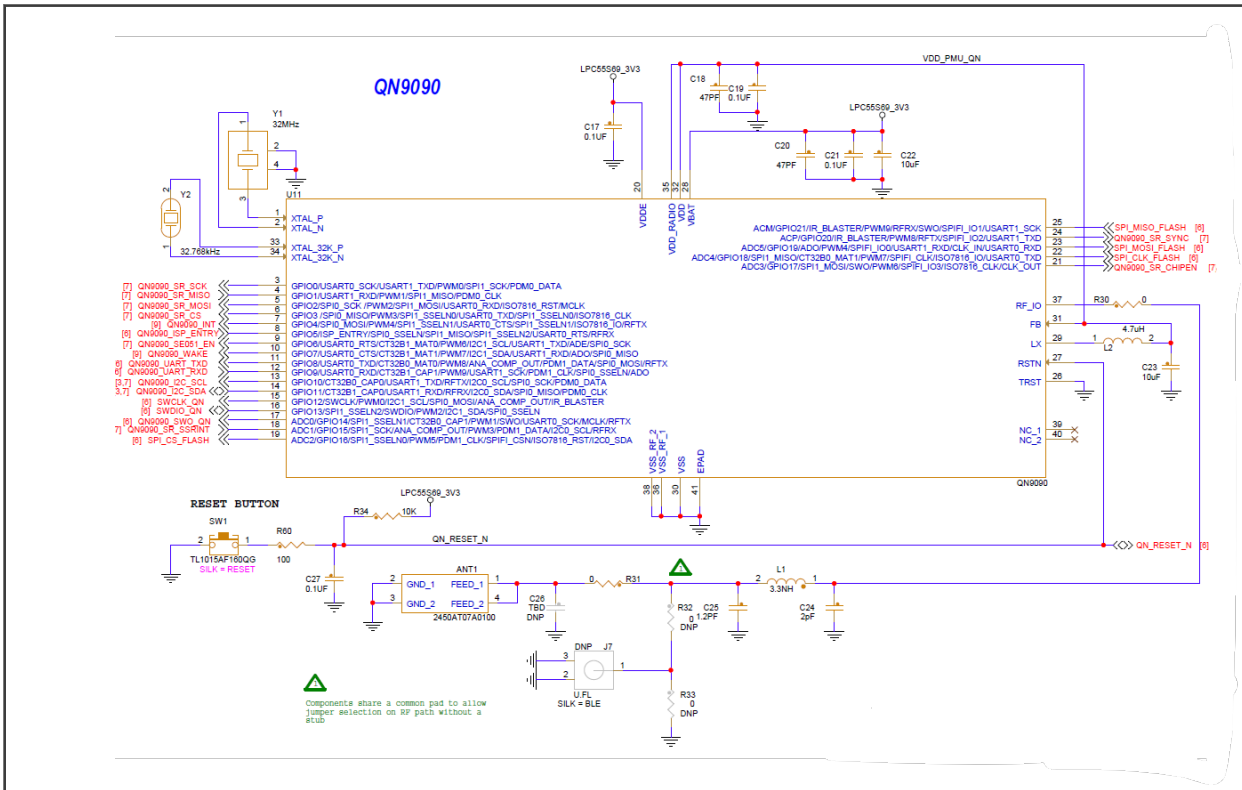


Figure 35. The schematic of QN9090 MCU on the FACECV board

Table 24. The QN9090 pin allocation in the FACECV board

J4 connector pin	QN9090 (pin)	Schematic net name
Pin 13	GPIO4	QN9090_INT
Pin 15	GPIO7	QN9090_WAKE

5.2 Memories

5.2.1 GD25Q32CSIG flash

One 32 Mbit/4 MB serial Quad SPI NOR flash memory GigaDevice GD25Q32CSIG is connected to the K32W061 MCU through its SPIFI interface in Quad SPI mode. This external memory stores the K32W061 application, which boots after reset, power cycle, or wake-up.

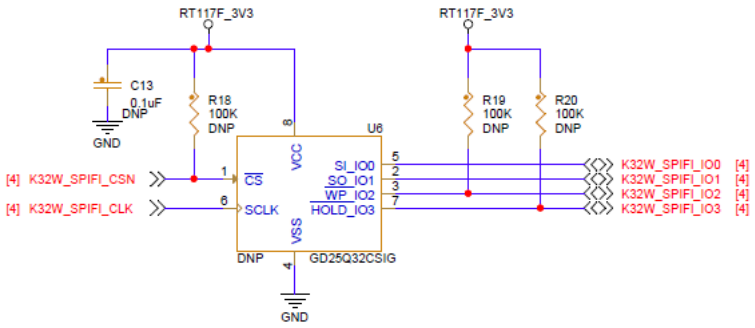


Figure 36. GD25Q32CSIG SPI NOR flash on the FACECV board

Table 25. GD25Q32CSIG pin allocation on the FACECV board

GD25Q32CSIG pin	OM15069-K32W module	Schematic net name
CS	PIO_16/SPIFI_CSN	K32W_SPIFI_CSN
SCLK	PIO_18/SPIFI_CLK	K32W_SPIFI_CLK
SI_IO0	PIO_19/SPIFI_IO0	K32W_SPIFI_IO0
SO_IO1	PIO_21_SPIFI_IO1	K32W_SPIFI_IO1
WP_IO2	PIO_20/SPIFI_IO2	K32W_SPIFI_IO2
HOLD_IO3	PIO_17/SPIFI_IO3	K32W_SPIFI_IO3

5.2.2 MX25R1635F flash

One 16 Mbit/2 MB ultra-low-power flash memory MX25R1635F is connected to the QN9090 MCU through its SPI interface. This external memory stores the QN9090 application, which boots after reset, power cycle, or wake-up.

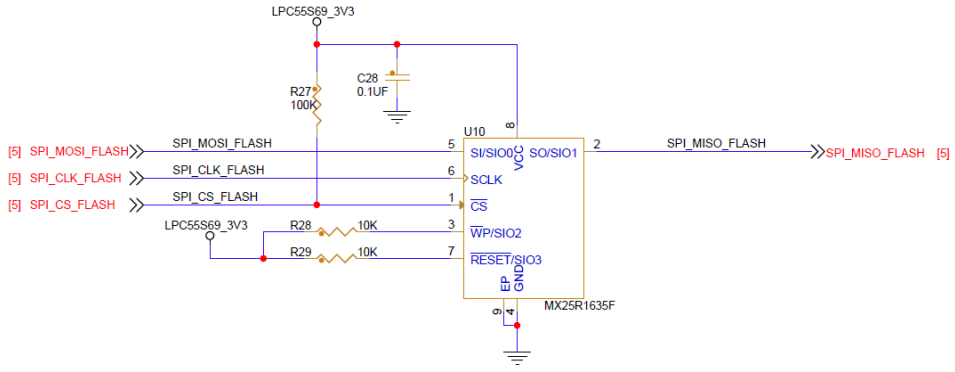


Figure 37. MX25R1635F SPI NOR flash on the FACECV board

Table 26. MX25R1635F pin allocation on the FACECV board

MX25R1635F pin	QN9090 MCU	Schematic net name
CS	GPIO16	SPI_CS_FLASH
SCLK	GPIO18	SPI_CLK_FLASH
SI/SIO0	GPIO19	SPI_MOSI_FLASH
SO/SIO1	GPIO21	SPI_MISO_FLASH
WP/SIO2	-	LPC55S69_3V3
RESET/SIO3	-	LPC55S69_3V3

5.3 Security

5.3.1 NXP SE051W

The FACECV board embeds an NXP SE051W security element, which supports applet updates in the field and delivers proven security certified to CC EAL 6+, with AVA_VAN.5 up to the OS level. It is connected to the LPC55S69 MCU located on the main board through the J4 connector or can be connected to the QN9090 MCU on the FACECV board.

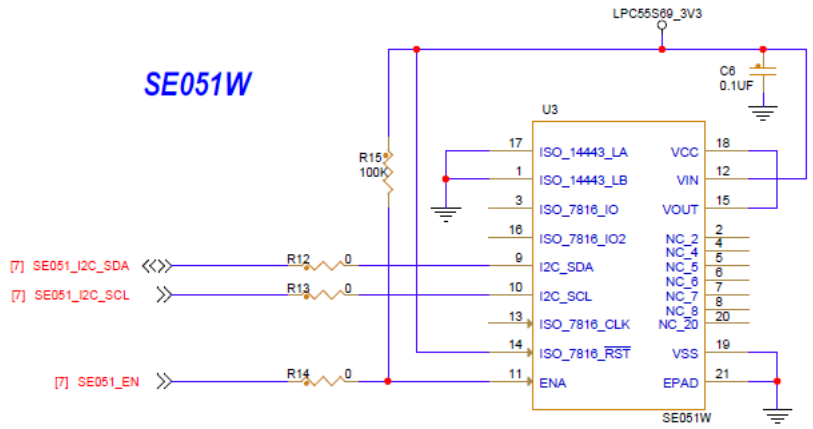


Figure 38. SE051W security element on the FACECV board

Table 27. SE051W pin allocation on the FACECV board

SE051W pin	J4 connector	QN9090 MCU	Schematic net name
I2C_SDA	LPC55_I2C_SDA	QN9090_I2C_SDA	SE051_I2C_SDA
I2C_SCL	LPC55_I2C_SCL	QN9090_I2C_SCL	SE051_I2C_SCL
ENA	LPC55_SE051_EN	QN9090_SE051_EN	SE051_EN

5.3.2 NXP SE051H

The FACECV board embeds an NXP SE051H security element. It is connected to the OM15069-K32W module through I2C interface and one ENABLE/DISABLE GPIO.

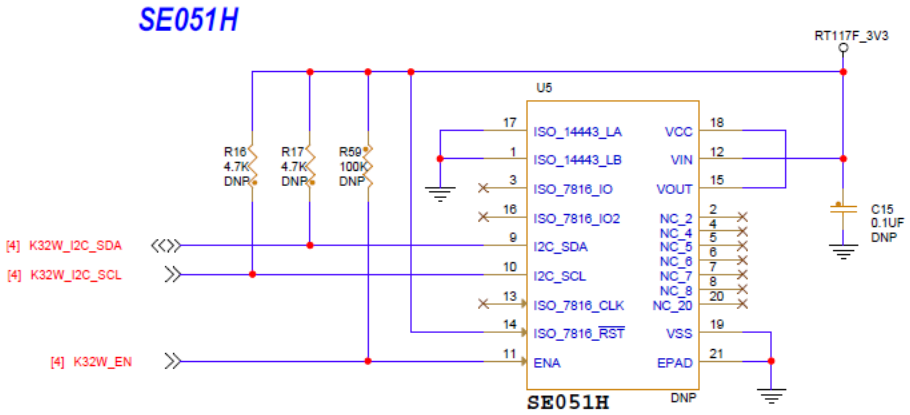


Figure 39. SE051H security element on the FACECV board

Table 28. SE051H pin allocation on the FACECV board

SE051H pin	OM15069-K32W module	Schematic net name
I2C_SDA	PIO_11/I2C0_SDA	K32W_I2C_SDA
I2C_SCL	PIO_10/I2C0_SCL	K32W_I2C_SCL
ENA	PIO_14/ADC0	K32W_EN

5.4 Connectors

J2 and J3 are 8-pin connectors connected to the SLN-VIZN3D-IOT kit. J4 is a 20-pin connector connected to the main board. The OM15069 K32W module is connected to the SLN-VIZN3D-IOT kit through J2 and J3 connectors. The main board is connected to the SLN-VIZN3D-IOT kit through J3 and J4 connectors. The signals of SWM1000SR150 are connected to the main board through the J4 connector.

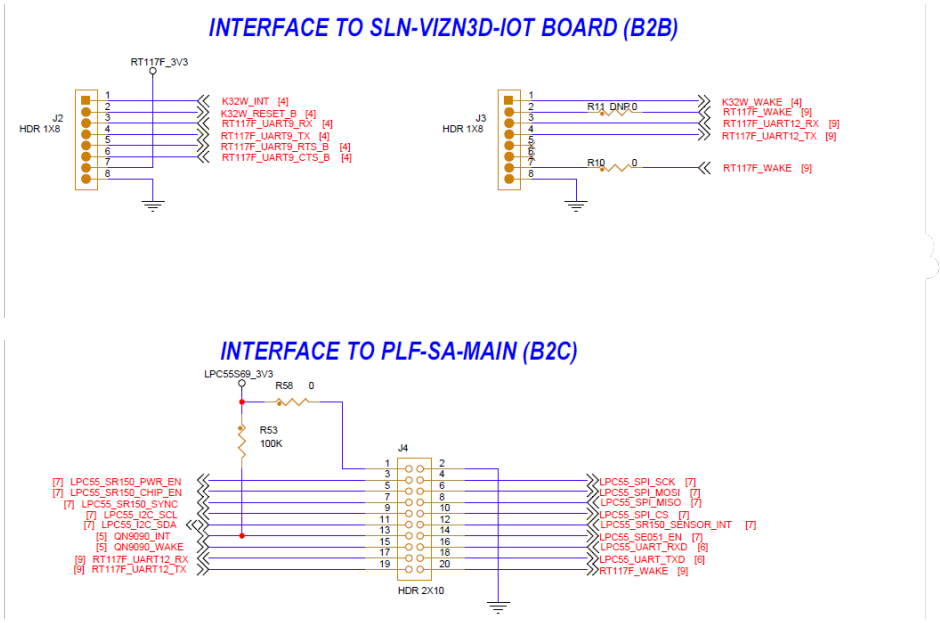


Figure 40. SE051H security element on the FACECV board

Chapter 6
Document Details

6.1 References

Below are listed the additional documents and resources that you can refer to for more information on the SLN-SMART-ACCESS kit. Some of the documents listed below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local NXP field applications engineer (FAE) or sales representative.

- SLN-SMART-ACCESS Home Page
- SLN-SMART-ACCESS User Guide
- SLN-SMART-ACCESS Software Guide

6.2 Acronyms, abbreviations, and definitions

Table 29. Acronyms and abbreviations

Term	Description
ADC	Analog-to-digital converter
DAC	Digital-to-analog converter
CAN	Controller Area Network
CSI	Camera Serial Interface
eMMC	Embedded Multimedia Card
GPIO	General Purpose In/Out
JTAG	Joint Test Access Group (IEEE® Std. 1149.1™)
LDO	Low Dropout Regulator
LED	Light Emitting Diode
MMC	Multi Media Card
MSD	Mass Storage Device
PLL	Phase-Locked Loop
QSPI	Quad Serial Peripheral Interface
ROM	Read-Only Memory
RTC	Real-time Clock
SD	Secure Digital Card

Table continues on the next page...

Table 29. Acronyms and abbreviations (continued)

SDHC	Secure Digital High Capacity
SRAM	Static Random Access Memory
SDRAM	Synchronous Dynamic Random-Access Memory
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

Chapter 7
Revision history

Table 30. Revision history

Date	Revision	Details of Change
07/04/22	1.0	Initial version

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